

(19) Japan Patent Office (JP)
(12) Japanese Unexamined Patent Application Publication (A)
(11) Japanese Unexamined Patent Application Publication Number S58-7903
(43) Publication Date: January 17, 1983

(51) Int. Cl.³
H03C 1/02
1/62

Identification No.

Internal Filing No.
7402-5J
7402-5J

Number of Inventions: 1
Application for Inspection: Filed

(Total 8 Pages)

(54) [Title of the Invention:] SWITCHED CAPACITOR MODULATOR

(21) Application No.: Japanese Patent Application S56-102176

(22) Application Filed: June 30, 1981

(72) Inventor:
John A. C. Bingham
2353 Webster Avenue
Palo Alto, California 94301
United States of America

(71) Applicant:
Racal Burdick Incorporated
222 Caspian Drive
Sunnyvale, California 94086

United States of America
(74) Agent:
Patent Attorney Kyouzou Yuasa
and one other individual

Specifications

1. (Title of the Invention)

SWITCHED CAPACITOR MODULATOR

2. (Scope of Patent Claims)

(1) A switched capacitor modulator that forms signals that are modulated by modulating carrier signals with modulated signals, comprising:

a primary capacitive medium that has first input to which the modulated signal is applied, second input to which a plurality of switching signals is applied, output that provides the sampled modulated signal, and first and second electrodes; and a switching means that contains a plurality of binary switches that connects said first and second electrodes to said input and output in response to the switching signals;

a logic means that generates said switching signals in response to a carrier signal and a clock signal that has frequency of at least four times that of the carrier signal;

and an integration means that provides a modulated signal in response to said sampled modulated signal.

(2) The modulator according to Claim 1 in the Scope of Patent Claims, wherein said plurality of binary switches includes at least first, second, third, and fourth switches; said first electrode is connected to said first input through the first switch and connected to the common ground through the second switch; and said second electrode is connected to said output through the third switch and connected to the common ground through the fourth switch.

(3) The modulator according to Claim 2 in the Scope of Patent Claims, wherein said logic means in the first half cycle of the carrier signal is configured such that said primary capacitive medium is charged with the modulated signal by generating switching signals that close said first and fourth switches and open said second and third switches in one of the half cycles of the clock signal, and said capacitive medium is discharged by generating switching signals that open said first and fourth switches and close said second and third switches in the remaining half cycle of the clock signal.

-7-

Japanese Unexamined Patent Application S58-7903 (2)

(4) The modulator according to Claim 3 in the Scope of Patent Claims, wherein said logic means in the second half cycle of the carrier signal is configured such that said primary capacitive medium is charged with the modulated signal by generating switching signals that close said first and third switches and open said second and fourth switches in one of the half cycles of the clock signal, and said capacitive medium is discharged by generating switching signals that open said first and third switches and close said second and fourth switches in the remaining half cycle of the clock signal.

(5) The modulator according to Claim 4 in the Scope of Patent Claims, wherein a delay means is established that consists of (1) an operational amplifier fifth switch that has input and output and (2) a storage capacitive medium; the input of the operational amplifier is connected to said first input through the fifth switch; the output of the operational amplifier is connected to said first switch; the storage capacitive medium is placed in between the input of the operational amplifier and the common ground, and it controls the fifth switch with a switching signal that is identical to that of the fourth switch.

(6) The modulator according to Claim 3 in the Scope of Patent Claims, wherein said switching means contains the fifth switch that connects said first input to said second electrode in response to switching signal S that is separate from those previously described; said logic means generates said switching signal S that opens this fifth switch in said first half cycle of the carrier signal; and said logic means in said second half cycle of the carrier signal further generates switching signals that charge said capacitive medium with a modulated signal by closing said second switch and opening said first and fourth switches, closing the fifth switch and opening the third switch in the first half cycle of the clock signal, and generates switching signals that discharge said capacitive medium by opening the fifth switch and closing the third switch in the second half cycle of the clock signal.

(7) The modulator according to Claim 3 in the Scope of Patent Claims, wherein said switching means contains the fifth switch that connects said output to said first electrode in response to switching signal S' that is separate from those previously described; said logic means generates said switching signal S' that opens this fifth switch in said first half cycle of the carrier signal; and said logic means in the second half cycle of the carrier signal further generates switching signals that charge said capacitive medium with a modulated signal by closing said fourth switch and opening said second and third switches, closing the first switch and opening the fifth switch in the first half cycle of the clock signal, and generates switching signals that discharge said capacitive medium by opening the first switch and closing the fifth switch in the second half cycle of the clock signal.

(8) The modulator according to Claim 5, Claim 6, or Claim 7 in the Scope of Patent Claims, wherein said switching means further contains a plurality of auxiliary capacitive media and a shaping medium that consists of a plurality of auxiliary switches that respond to auxiliary switching signals; each auxiliary capacitive medium is connected to both ends of said primary capacitive medium through the corresponding auxiliary switch; and said logic means generates said auxiliary switching signals that activate said auxiliary switches with a frequency that is an integer multiple of that of the carrier signal.

3. (Detailed Description of the Invention)

The present invention is related to technology that modulates signals by crossing a signal from a given frequency range with a signal from a second frequency range that is between an approximate sinusoidal wave and a square wave.

In the past, modulators were constructed by combining various nonlinear devices – vacuum tubes, diodes, transistors, and switches, for example – with a transformer or an amplifier. For example, the modulator shown in US Patent Number 3,937,882 (Bingham, dated February 10, 1976) can be considered a case in point of such devices. As requirements from the standpoint of design, if it were necessary to restrain the values that correspond to all of the spurious output of the modulator to extremely low values, it was generally considered necessary to regulate the circuit parameters individually.

It is often desired to implement the transfer functions of electronic circuits with only the components that can be mounted to the LSI circuit.